What is claimed is:

1. A method of creating metal gate electrodes and polysilicon gate electrodes over the surface of a substrate, said metal gate electrodes and said polysilicon gate electrodes having gate dielectric layers of different thicknesses, comprising the steps of:

providing a semiconductor substrate, at least one first and one second gate electrode structures having been provided over the surface of said substrate, said at least one first and said at least one second gate electrode having been provided with a gate electrode body having a surface further having sidewalls which are essentially perpendicular to the surface of said substrate, said at least one first and said at least one second gate electrode having been provided with Lightly Doped Diffusion impurity implants into the surface of said substrate that are self-aligned with the body of said at least one first and said at least one second gate electrode, said at least one first and said at least one second gate electrode having been provided with gate spacers over said sidewalls of said at least one first and said at least one second gate electrode, said at least one first and said at least one second gate electrode having been provided with source and drain impurity implants into the surface of said substrate that are self-aligned with the gate spacers of said at least one first and said at least one second gate electrode, said

at least one first and said at least one second gate electrode being imbedded in a layer of Intra Metal Dielectric (IMD), said layer of IMD having been polished down to the surface of the body of said at least one first and said at least one second gate electrode, said at least one first and said at least one second gate electrode being electrically isolated from each other by a region of Field Isolation that has been created in the surface of said substrate;

creating a photoresist mask overlying said at least one second gate electrode;

removing said dummy gate electrode from between said gate spacers of said at least one first gate electrode, creating at least one opening in said layer of IMD;

depositing a layer of high-k dielectric over the surface of said layer of IMD, including inside surfaces of said at least one opening created in said layer of IMD;

depositing a layer of metal over the surface of said layer of high-k dielectric, filling said at least one opening created in said layer of IMD; and

removing said layer of high-k dielectric and said layer of metal from above the surface of said layer of IMD, leaving said layer of high-k dielectric in place over inside surfaces of said at least one opening created in said layer of IMD, further leaving said layer of metal in place over the surface of said

layer of high-k dielectric inside said at least one opening created in said layer of IMD.

2. The method of claim 1 wherein said layer of high-k dielectric deposited over the surface of said layer of IMD is deposited to a thickness of between about 50 and 150 Angstrom and more preferably to a thickness of about 100 Angstrom.

3. The method of claim 1 wherein said layer of high-k dielectric deposited over the surface of said layer of IMD is selected from the group consisting of silicon nitride (Si_3N_4) and aluminum oxide (Al_2O_3) and oxide-nitride-oxide (ONO) and silicon oxide (Si_2O) and tantalum pentoxide (TaO_5) and titanium oxide (TiO_2) and zirconium oxide (ZrO_2) and tantalum oxide (Ta_2O_5) and barium titanium oxide ($BaTiO_3$) and strontium titanium oxide ($SrTiO_3$).

4. The method of claim 1 wherein said layer of metal deposited over the surface of said layer of high-k comprises a metal selected from the group consisting of titanium and tungsten and copper and aluminum and alloys thereof.

5. The method of claim 1 wherein said gate electrode body of said at least one first gate electrode comprises a patterned layer of

gate dielectric created over the surface of said substrate over which a patterned layer of polysilicon has been created.

6. The method of claim 1 wherein said gate electrode body of said at least one second gate electrode comprises a patterned layer of gate dielectric deposited to a thickness between about 300 and 600 Angstrom and more preferably about 450 Angstrom over which a patterned layer of polysilicon has been created.

7. The method of claim 1 with an additional processing step of depositing a layer of barrier material over the surface of said layer of IMD, said additional processing step being performed prior to depositing said high-k dielectric over the surface of said layer of IMD, said layer of barrier material being removed from the surface of said layer of IMD as an extension of said step of removing said layer of high-k dielectric and said layer of metal from above the surface of said layer of IMD, leaving said barrier material in place overlying inside surfaces of said at least one opening created in said layer if IMD.

8. The method of claim 1 with additional processing steps of saliciding contact surfaces to said at least one first and said at least one second gate electrode, said salicidation being performed prior to said providing gate spacers over said

sidewalls of said at least one first and said at least one second gate electrode.

9. A method of creating at least one high voltage polysilicon gate electrode and one low voltage metal gate electrode over the surface of a substrate, comprising the steps of:

providing a semiconductor substrate;

creating a region of Field Isolation in the surface of said substrate, thereby separating an active surface region in the surface of said substrate over which said at least one high-voltage gate electrode is to be created from an active surface region in the surface of said substrate over which said at least one low-voltage metal gate electrode is to created;

creating a layer of gate oxide over the surface of said substrate, said layer of gate oxide having a thickness between about 300 and 600 Angstrom and more preferably about 450 Angstrom;

depositing a layer of polysilicon over the surface of said layer of gate oxide;

patterning and etching said layer of polysilicon and said layer of pad oxide, creating patterned layers of polysilicon and gate oxide having sidewalls further having a surface for said at least one high voltage polysilicon gate electrode and said at

least one low voltage metal gate electrode over the surface of a substrate;

performing Lightly Doped Diffusion impurity implants into the surface of said substrate self-aligned with said patterned layers of polysilicon and gate oxide for said at least one high voltage polysilicon gate electrode and said at least one low voltage metal gate electrode;

creating gate spacers over sidewalls of said patterned layers of polysilicon and gate oxide for said at least one high voltage polysilicon gate electrode and said at least one low voltage metal gate electrode;

performing source and drain impurity implants into the surface of said substrate self-aligned with said gate spacers created over sidewalls of said patterned layers of polysilicon and gate oxide for said at least one high voltage polysilicon gate electrode and said at least one low voltage metal gate electrode;

saliciding the surface of said source and drain impurity implants and the surface of said patterned layers of polysilicon for said at least one high voltage polysilicon gate electrode and said at least one low voltage metal gate electrode, creating salicided contact surfaces to said at least one high voltage polysilicon gate electrode and said at least one low voltage metal gate electrode;

depositing a layer of Intra Metal Dielectric over the surface of said substrate, including the salicided contact surfaces and the surface of said gate spacers created over sidewalls of said patterned layers of polysilicon and gate oxide for said at least one high voltage polysilicon gate electrode and said at least one low voltage metal gate electrode;

polishing said deposited layer of Intra Metal Dielectric down to said salicided contact surfaces of said patterned and salicided layers of polysilicon for said at least one high voltage polysilicon gate electrode and said at least one low voltage metal gate electrode;

creating a photoresist mask overlying the surface of said layer of Intra Metal Dielectric, said photoresist mask overlying said at least one high voltage polysilicon gate electrode;

removing said at least one low voltage gate electrode from between said gate spacers formed over sidewalls of said patterned layers of polysilicon and gate oxide for said at least one low voltage polysilicon gate electrode, creating at least one opening in said layer of IMD;

depositing a layer of high-k dielectric over the surface of said layer of IMD, including inside surfaces of said at least one opening created in said layer of IMD;

depositing a layer of metal over the surface of said layer of high-k dielectric, filling said at least one opening created in said layer of IMD; and

removing said layer of high-k dielectric and said layer of metal from above the surface of said layer of IMD, leaving said layer of high-k dielectric in place over inside surfaces of said at least one opening created in said layer of IMD, further leaving said layer of metal in place over the surface of said layer of high-k dielectric inside said at least one opening created in said layer of IMD.

10. The method of claim 9 wherein said layer of high-k dielectric deposited over the surface of said layer of IMD is deposited to a thickness of between about 50 and 150 Angstrom and more preferably to a thickness of about 100 Angstrom.

11. The method of claim 9 wherein said layer of high-k dielectric deposited over the surface of said layer of IMD is selected from the group consisting of silicon nitride (Si_3N_4) and aluminum oxide (Al_2O_3) and oxide-nitride-oxide (ONO) and silicon oxide (Si_2O) and tantalum pentoxide (TaO_5) and titanium oxide (TiO_2) and zirconium oxide (ZrO_2) and tantalum oxide (Ta_2O_5) and barium titanium oxide ($BaTiO_3$) and strontium titanium oxide ($SrTiO_3$).

12. The method of claim 9 wherein said layer of metal deposited over the surface of said layer of high-k comprises a metal selected from the group consisting of titanium and tungsten and copper and aluminum and alloys thereof.

13. The method of claim 9 wherein said at least one high voltage polysilicon gate electrode comprises a patterned layer of gate dielectric deposited to a thickness between about 300 and 600 Angstrom and more preferably about 450 Angstrom over which a patterned and salicided layer of polysilicon has been created.

14. The method of claim 9 with an additional processing step of depositing a layer of barrier material over the surface of said layer of IMD, said additional processing step being performed prior to depositing said high-k dielectric over the surface of said layer of IMD, said layer of barrier material being removed from the surface of said layer of IMD as an extension of said step of removing said layer of high-k dielectric and said layer of metal from above the surface of said layer of IMD, leaving said barrier material in place overlying inside surfaces of said at least one opening created in said layer if IMD.